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			02/20/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/587,744

Applicant(s)

YAMAZAKI ET AL.

Examiner

MICHELE FAN

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 January 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) See Continuation Sheet is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 7/28/09 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 7/28/06, 9/18/06, 10/9/08
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

Continuation of Disposition of Claims: Claims pending in the application are 2,3,5-7,9,10,12,13,15,16,18,19,21,22,24,25,27,28,30,31,33,34,36,37,39,40,42,43,45 and 46.

Continuation of Disposition of Claims: Claims rejected are 2,3,5-7,9,10,12,13,15,16,18,19,21,22,24,25,27,28,30,31,33,34,36,37,39,40,42,43,45 and 46.

DETAILED ACTION

Election/Restrictions

Applicant's election of Invention II (method of manufacturing a thin film integrated circuit with a connection region), claims 2, 3, 5-7, 9, 10, 12, 13, 15, 16, 18, 19, 21, 22, 24, 25, 27, 28, 30, 31, 33, 34, 36, 37, 39, 40, 42, 43, 45, 46 in the reply filed on January 8, 2009 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's cancellation of claims 1, 4, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44 in the reply filed on January 8, 2009 is acknowledged.

Specification

Receipt is acknowledged of a certified copy of the JP 2004-031064 filed on February 6, 2004 application referred to in the oath or declaration or in an application data sheet. If this copy is being filed to obtain the benefits of the foreign filing date under 35 U.S.C. 119(a)-(d), applicant should also file a claim for such priority as required by 35 U.S.C. 119(b). If the application being examined is an original application filed under 35 U.S.C. 111(a) (other than a design application) on or after November 29, 2000, the claim for priority must be presented during the pendency of the application, and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. See 37 CFR 1.55(a)(1)(i). If the application being examined has entered the national stage

from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the claim for priority must be made during the pendency of the application and within the time limit set forth in the PCT and Regulations of the PCT. See 37 CFR 1.55(a)(1)(ii). Any claim for priority under 35 U.S.C. 119(a)-(d) or (f) or 365(a) or (b) not presented within the time period set forth in 37 CFR 1.55(a)(1) is considered to have been waived. If a claim for foreign priority is presented after the time period set forth in 37 CFR 1.55(a)(1), the claim may be accepted if the claim properly identifies the prior foreign application and is accompanied by a grantable petition to accept an unintentionally delayed claim for priority. See 37 CFR 1.55(c).

Examiner notes that a claim to foreign priority is missing from the first line of the specification. (An incorporation by reference to JP 2004-031064 is on the /last page of the specification.)

Claim Rejections - 35 USC § 102

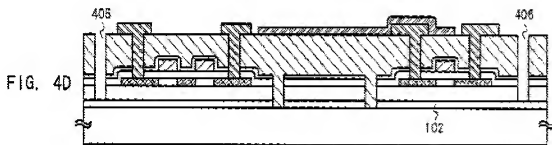
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

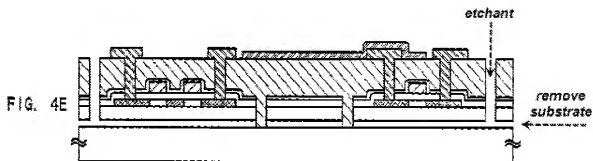
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2, 12, 15, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al., US Publication No. 2001/0015256 A1 (from the International Search Report).

(see fig. 4D) **selectively forming a groove (405, 406) between the two thin film integrated circuits to expose a part of the separation layer (102) and form a connection region which is a part of the two thin film integrated circuits; and**



(see fig. 4E) separating the insulating substrate by introducing an etchant into the opening and removing the separation layer, pg. 4, ¶ 51-57;



wherein the two thin film integrated circuits are integrated by the connection region, pg. 2, ¶ 23-32, pg. 4, ¶ 51-57, fig. 1A-1D, 4A-4E;

limitations from claim 12 the method for manufacturing a thin film integrated circuit according to claim 2,

wherein the etchant is a gas or a liquid including halide typified by ClF_3 , limitation: ClF_3 , pg. 4, ¶ 55;

limitations from claim 15, the method for manufacturing a thin film integrated circuit according to claim 2,

wherein the insulating substrate is a glass substrate, a quartz substrate, or a substrate made of a synthetic resin such as plastic or acrylic, limitation: quartz, pg. 2, ¶ 24;

limitations from claim 27, the method for manufacturing a thin film integrated circuit according to claim 2,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor, limitation: amorphous semiconductor (amorphous silicon film), pg. 2, ¶ 24;

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 7, 10, 13, 16, 24, 28, 31, 34, 37, 40, 43 rejected under 35 U.S.C.

103(a) as being unpatentable over Yamazaki and Jurisch, US Patent No. 5, 308,967.

Yamazaki teaches:

limitations from claim 3, a method for manufacturing a thin film integrated circuit, comprising the steps of:

(see fig. 1A and 1D above) forming a separation layer (102) over an insulating substrate;

forming at least two thin film integrated circuits (201, 202) over the separation layer, pg. 2, ¶ 23-32;

(see fig. 4D above) selectively forming a groove (405, 406) between the two thin film integrated circuits to expose a part of the separation layer (102) and form a connection region which is a part of the two thin film integrated circuits;

(see fig. 4E above) separating the insulating substrate by introducing an etchant into the groove and the opening and removing the separation layer, pg. 4, ¶ 51-57;

wherein the two thin film integrated circuits are integrated by a fixed substrate (130), pg. 3, ¶ 41-42, pg. 4, ¶ 59, fig. 2A:

Yamazaki lacks an antenna substrate.

Jurisch teaches:

(see fig. 1) attaching an antenna substrate (3) provided with an opening and an antenna (2) over the two (one) thin film integrated circuits (1a, 1b- polysilicon gate and diffusion area), Abstract, col. 2, ln 10-34, ln 59-67, col. 3, ln 1-15, fig. 1:

Note: In fig. 1, Jurisch discloses an antenna coil (2) formed over a bulk semiconductor material. The bulk semiconductor material comprises a diffusion area (1a), a polysilicon gate (1b), insulating layers (1c, 1d), conductive path (1e), and passivation layer (1f).

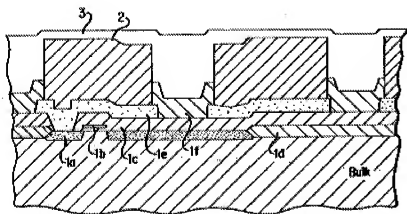


FIG. 1

Yamazaki further teaches:

limitations from claim 7, the method for manufacturing a thin film integrated circuit according to claim 3, further comprising the step of:

attaching the two thin film integrated circuits to a flexible substrate (132), pg. 4, ¶ 61, fig. 5C:

limitations from claim 10, the method for manufacturing a thin film integrated circuit according to claim 3,

wherein each of the thin film integrated circuits comprises a thin film transistor (201, switch TFT and 202, control TFT) and an insulating film containing nitrogen provided over (silicon nitride film) and under (103, silicon oxide film) the thin film transistor, pg. 2, ¶ 26-30, fig. 1C;

Yamazaki discloses the claimed invention except for forming an insulating film containing nitrogen under the thin film transistor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a insulating film containing nitrogen under the thin film transistor, since it has been held to be within the general skill of a worker in the art to select known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. See MPEP § 2144.07, Art Recognized Suitability for an Intended Purpose.

limitations from claim 13, the method for manufacturing a thin film integrated circuit according to claim 3,

wherein the etchant is a gas or a liquid including halide typified by ClF_3 , limitation: ClF_3 , pg. 4, ¶ 55;

limitations from claim 16, the method for manufacturing a thin film integrated circuit according to claim 3,

wherein the insulating substrate is a glass substrate, a quartz substrate, or a substrate made of a synthetic resin such as plastic or acrylic, limitation: quartz, pg. 2, ¶ 24;

Jurisch further teaches:

limitations from claim 24, the method for manufacturing a thin film integrated circuit according to claim 3,

wherein the antenna is formed by a method selected from the group consisting of a droplet discharge method, a sputtering method, a printing method, a plating method, a

photolithography method, an evaporation method using a metal mask, and a combination thereof, limitation: plating method, pg. 2, ¶ 59-67, pg. 3, ¶ 1-15;

Yamazaki further teaches:

limitations from claim 28, the method for manufacturing a thin film integrated circuit according to claim 3,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor, limitation: amorphous semiconductor (amorphous silicon film), pg. 2, ¶ 24;

limitations from claim 31, the method for manufacturing a thin film integrated circuit according to claim 3,

wherein the two thin film integrated circuits (201, 202) have a thickness of 0.3 μm to 3 μm , pg. 2, ¶ 26-32;

Yamazaki discloses the claimed invention except for indicating the thin film transistors have a thickness of 0.3-3 μm . It would have been obvious to one having ordinary skill in the art at the time the invention was made to form thin film transistors with a thickness of 0.3-3 μm , since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05, Optimization of Ranges.

limitations from claim 34, the method for manufacturing a thin film integrated circuit according to claim 3,

wherein the two thin film integrated circuits (201, 202) are 5 mm squared or less, pg. 2, ¶ 26-32;

Yamazaki discloses the claimed invention except for indicating the thin film transistors are 5 mm squared or less. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form thin film transistors that are 5 mm

squared or less, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05, Optimization of Ranges.

limitations from claim 37, the method for manufacturing a thin film integrated circuit according to claim 3,

wherein each of the two thin film integrated circuits (201, 202) includes a semiconductor film having a hydrogen concentration of $1 \times 10^{19}/\text{cm}^3$ to $5 \times 10^{20}/\text{cm}^3$, pg. 2, ¶ 30;

Yamazaki discloses a hydrogenation treatment is performed by a hydrogen annealing or plasma hydrogenation technique. Examiner notes it is possible for one having ordinary skill in the art to measure the hydrogen concentration in the semiconductor film after hydrogenation treatment.

Yamazaki discloses the claimed invention except for indicating the thin film transistors have a hydrogen concentration of $1 \times 10^{19}/\text{cm}^3$ to $5 \times 10^{20}/\text{cm}^3$. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form thin film transistors have a hydrogen concentration of $1 \times 10^{19}/\text{cm}^3$ to $5 \times 10^{20}/\text{cm}^3$, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05, Optimization of Ranges.

limitations from claim 40, the method for manufacturing a thin film integrated circuit according to claim 37,

wherein the semiconductor film (104) has a thickness of 0.2 μm or less, (50 nm or 0.05 μm), pg. 2, ¶ 26;

limitations from claim 43, the method for manufacturing a thin film integrated circuit according to claim 37,

wherein the semiconductor film (104) comprises a source region, a drain region, (110/114 are source/drain regions) and a channel formation region (115/117) and, pg. 2, ¶ 27-28:

Yamazaki lacks:

wherein the source region, the drain region, and the channel formation region are formed to be perpendicular to a bending direction of a mount article;

Yamazaki discloses the claimed invention except for indicating the source, drain, and channel regions are formed to be perpendicular to a bending direction of a mount article
It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the source, drain, and channel regions perpendicular to a bending direction of a mount article since it was known in the art that an integrated circuit formed perpendicular to the bending direction of a mount article enables a greater surface area of the integrated circuit (and the antenna formed thereon) to communicate with an external device.

Jurisch provides motivation in col. 1, ln 45-65.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Jurisch's invention with Yamazaki's invention would have been beneficial because integrating circuits and an antenna on a single chip eliminates the otherwise expensive mounting and connection of individual components. The reliability is thereby increased and the geometry of the data carrier is considerably minimized.

Claims 5, 6, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki and Jurisch.

Yamazaki teaches limitations from claim 2, a method for manufacturing a thin film integrated circuit, comprising forming a separation layer for a substrate; forming at least two thin film integrated circuits; and forming a groove to introduce an etchant for removing the separation layer.

Yamazaki lacks an antenna.

Jurisch teaches:

limitations from claim 5, the method for manufacturing a thin film integrated circuit according to claim 2, further comprising the step of:

(see fig. 1 above) **attaching an antenna (2) to the two thin film integrated circuits (1a, 1b- polysilicon gate and diffusion area), Abstract, col. 2, ln 10-34, ln 59-67, col. 3, ln 1-15, fig. 1;**

Note: In fig. 1, Jurisch discloses an antenna coil (2) formed over a bulk semiconductor material. The bulk semiconductor material comprises a diffusion area (1a), a polysilicon gate (1b), insulating layers (1c, 1d), conductive path (1e), and passivation layer (1f).

Yamazaki teaches:

limitations from claim 6, the method for manufacturing a thin film integrated circuit according to claim 2, further comprising the steps of:

attaching the two thin film integrated circuits to a flexible substrate (132), pg. 4, ¶ 61, fig. 5C;

Yamazaki lacks an antenna.

Jurisch teaches:

attaching an antenna to the two thin film integrated circuits, as applied to claim 5 above;

Jurisch further teaches:

limitations from claim 25, the method for manufacturing a thin film integrated circuit according to claim 5,

wherein the antenna is formed by a method selected from the group consisting of a droplet discharge method, a sputtering method, a printing method, a plating method, a photolithography method, an evaporation method using a metal mask, and a combination thereof, limitation: plating method, pg. 2, ¶ 59-67, pg. 3, ¶ 1-15;

Claims 9, 30, 33, 36, 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki, as applied to claim 2 above.

Yamazaki teaches limitations from claim 2, a method for manufacturing a thin film integrated circuit, comprising forming a separation layer for a substrate; forming at least two thin film integrated circuits; and forming a groove to introduce an etchant for removing the separation layer.

Yamazaki further teaches:

limitations from claim 9, the method for manufacturing a thin film integrated circuit according to claim 2,

wherein each of the thin film integrated circuits comprises a thin film transistor (201, switch TFT and 202, control TFT) and an insulating film containing nitrogen provided over (silicon nitride film) and under (103, silicon oxide film) the thin film transistor, pg. 2, ¶ 26-30, fig. 1C;

Yamazaki discloses the claimed invention except for forming an insulating film containing nitrogen under the thin film transistor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a insulating film containing nitrogen under the thin film transistor, since it has been held to be within the general skill of a worker in the art to select known material on the basis of its

suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. See MPEP § 2144.07, Art Recognized Suitability for an Intended Purpose.

limitations from claim 30, the method for manufacturing a thin film integrated circuit according to claim 2,

wherein the two thin film integrated circuits (201, 202) have a thickness of 0.3 μ m to 3 μ m, pg. 2, ¶ 26-32;

Yamazaki discloses the claimed invention except for indicating the thin film transistors have a thickness of 0.3-3 μ m. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form thin film transistors with a thickness of 0.3-3 μ m, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05, Optimization of Ranges.

limitations from claim 33, the method for manufacturing a thin film integrated circuit according to claim 2,

wherein the two thin film integrated circuits (201, 202) are 5 mm squared or less, pg. 2, ¶ 26-32;

Yamazaki discloses the claimed invention except for indicating the thin film transistors are 5 mm squared or less. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form thin film transistors that are 5 mm squared or less, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05, Optimization of Ranges.

limitations from claim 36, the method for manufacturing a thin film integrated circuit according to claim 2,

wherein each of the two thin film integrated circuits (201, 202) includes a semiconductor film having a hydrogen concentration of $1 \times 10^{19}/\text{cm}^3$ to $5 \times 10^{20}/\text{cm}^3$, pg. 2, ¶ 30:

Yamazaki discloses a hydrogenation treatment is performed by a hydrogen annealing or plasma hydrogenation technique. Examiner notes it is possible for one having ordinary skill in the art to measure the hydrogen concentration in the semiconductor film after hydrogenation treatment.

Yamazaki discloses the claimed invention except for indicating the thin film transistors have a hydrogen concentration of $1 \times 10^{19}/\text{cm}^3$ to $5 \times 10^{20}/\text{cm}^3$. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form thin film transistors have a hydrogen concentration of $1 \times 10^{19}/\text{cm}^3$ to $5 \times 10^{20}/\text{cm}^3$, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05, Optimization of Ranges.

limitations from claim 39, the method for manufacturing a thin film integrated circuit according to claim 36,

wherein the semiconductor film (104) has a thickness of 0.2 μm or less, (50 nm or 0.05 μm), pg. 2, ¶ 26:

limitations from claim 42, the method for manufacturing a thin film integrated circuit according to claim 36,

wherein the semiconductor film (104) comprises a source region, a drain region, and a channel formation region (110/114 are source/drain regions) and, pg. 2, ¶ 27-28:

Yamazaki lacks:

wherein the source region, the drain region, and the channel formation region are formed to be perpendicular to a bending direction of a mount article;

Yamazaki discloses the claimed invention except for **indicating the source, drain, and channel regions are formed to be perpendicular to a bending direction of a mount article**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to **form the source, drain, and channel regions perpendicular to a bending direction of a mount article** since it was known in the art that **an integrated circuit formed perpendicular to the bending direction of a mount article enables a greater surface area of the integrated circuit (and the antenna formed thereon) to communicate with an external device.**

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki and Ikefuji et al., US Patent No. 6,422,473 B1.

Yamazaki teaches limitations from claim 2, a method for manufacturing a thin film integrated circuit, comprising forming a separation layer for a substrate; forming at least two thin film integrated circuits; and forming a groove to introduce an etchant for removing the separation layer.

Yamazaki lacks mounting the two thin film integrated circuits on a mount article and a mount position.

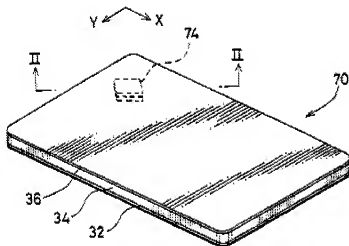
Ikefuji teaches:

limitations from claim 18, the method for manufacturing a thin film integrated circuit according to claim 2,

(see fig. 1) wherein a mounting position of each of the two thin film integrated circuits X satisfies $X \mu\text{m}$ when a thickness of a mount article is denoted by D, col. 1, ln 1-10, col. 2, ln 10-18, fig. 1;

In fig. 1, Ikefuji teaches mounting an integrated circuit on a card. The IC card can be used for the gate of the ski lift, the gate at the station, and automatic sorting of parcels and the like.

FIG. 1



Ikefuji lacks wherein a mounting position of X satisfies $(1/2)D-30 \mu\text{m} < X < (1/2)D+30 \mu\text{m}$.

Ikefuji discloses the claimed invention except for indicating the mount position X satisfies $(1/2)D-30 \mu\text{m} < X < (1/2)D+30 \mu\text{m}$. It would have been obvious to one having ordinary skill in the art at the time the invention was made to mount an IC on an article with a position X that satisfies $(1/2)D-30 \mu\text{m} < X < (1/2)D+30 \mu\text{m}$, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. See MPEP § 2144.05, Optimization of Ranges.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Ikefuji's invention with Yamazaki's invention would have been beneficial because mounting an integrated circuit on an a card allows for portability and remote access functions.

Claims 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki and Jurisch as applied to claims 2 and 3 above, and further in view of Ikefuji.

Yamazaki and Jurisch teach limitations from claim 2 and 5, a method for manufacturing a thin film integrated circuit, comprising forming a separation layer for a substrate; forming at least two thin film integrated circuits; and forming a groove to introduce an enchan for removing the separation layer. An antenna is attached to the two thin film integrated circuits.

Yamazaki and Jurisch teach limitations from claim 3, a method for manufacturing a thin film integrated circuit, comprising forming a separation layer for a substrate; forming at least two thin film integrated circuits; forming a groove; forming an antenna substrate thereon; and introducing an enchan into the groove for removing the separation layer.

Yamazaki lacks mounting the two thin film integrated circuits on a mount article and a mount position.

Ikefuji teaches:

limitations from claim 19, the method for manufacturing a thin film integrated circuit according to claim 3,

(see fig. 1 above) wherein a mounting position of each of the two thin film integrated circuits X satisfies $X \mu\text{m}$ when a thickness of a mount article is denoted by D, col. 1, ln 1-10, col. 2, ln 10-18, fig. 1;

In fig. 1, Ikefuji teaches mounting an integrated circuit on a card. The IC card can be used for the gate of the ski lift, the gate at the station, and automatic sorting of parcels and the like.

Ikefuji lacks wherein a mounting position of X satisfies $(1/2)D-30 \mu\text{m} < X < (1/2)D+30 \mu\text{m}$.

Ikefuji discloses the claimed invention except for indicating the mount position X satisfies $(1/2)D-30 \mu\text{m} < X < (1/2)D+30 \mu\text{m}$. It would have been obvious to one having ordinary skill in the art at the time the invention was made to mount an IC on an article with a position X that satisfies $(1/2)D-30 \mu\text{m} < X < (1/2)D+30 \mu\text{m}$, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. See MPEP § 2144.05, Optimization of Ranges.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Ikefuji's invention with Yamazaki and Jurisch's invention would have been beneficial because mounting an integrated circuit on an a card allows for portability and remote access functions.

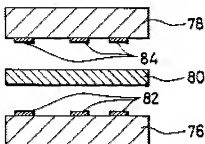
Jurisch teaches:

limitations from claims 21 and 22, the method for manufacturing a thin film integrated circuit according to claims 3 and 5,

(see fig. 3B) wherein the antenna (on IC chip 76) is attached to the two thin film integrated circuits (76, 78) by an anisotropic conductor (80), an ultrasonic adhesive, or an ultraviolet curing resin, limitation: anisotropic conductor, Abstract, col. 2, ln 10-27, ln 47-54, col. 3, ln 19-37, col. 5, ln 10-49, fig. 1, 2, 3A-3B;

In. fig. 3B, Ikefuji teaches attaching IC chips with an anisotropic conductor. Ikefuji indicates an anisotropic conductor is a conductor having conductivity only in one direction and provides adhesion.

FIG. 3B



Ikefuji provides motivation in col. 2, In 47-54, col. 3, In 22-37.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Ikefuji's invention with Yamazaki and Jurisch's invention would have been beneficial because using an anisotropic conductor enables a connection to be achieved without an external arrangement of an interconnection, thereby facilitating manufacturing assembly processes.

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki and Kawamura et al., US Patent No. 7,129,145 (from Information Disclosure Statement).

Yamazaki teaches limitations from claim 2, a method for manufacturing a thin film integrated circuit, comprising forming a separation layer for a substrate; forming at least

two thin film integrated circuits; and forming a groove to introduce an etchant for removing the separation layer.

Yamazaki lacks cutting the two thin film integrated circuits.

Kawamura teaches:

limitations from claim 45, the method for manufacturing a thin film integrated circuit according to claim 2,

(see fig. 6 and 1B) wherein a thin film integrated circuit is formed by cutting the two thin film integrated circuits by a dicing, a scribing, or a laser cutting method, limitation: scribing, col. 6, ln 10-22, col. 7, ln 31-67, col. 8, ln 1-16, col. 9, ln 1-41, fig. 1B and 6:

In fig. 6, Kawamura teaches a plurality of IC elements (1) are formed on a wafer (11). Antenna coils (3) are formed on top of the IC elements. The wafer is scribed to form individual IC elements as shown in fig. 1B.

FIG. 6

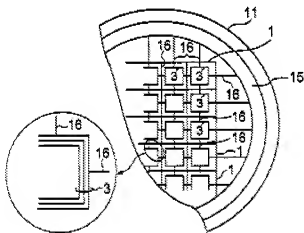
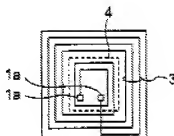


FIG. 1B



Kawamura provides motivation in col. 9, ln 1-41.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Kawamura's invention with Yamazaki's invention would have been beneficial because the IC elements each formed integrally with the coil can be manufactured with high efficiency at lower manufacturing cost when compared with the case where the individual coils are each formed on the individual IC elements, respectively.

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki and Jurisch as applied to claim 3 above, and further in view of Kawamura.

Yamazaki and Jurisch teach limitations from claim 3, a method for manufacturing a thin film integrated circuit, comprising forming a separation layer for a substrate; forming at least two thin film integrated circuits; forming a groove; forming an antenna substrate thereon; and introducing an etchant into the groove for removing the separation layer.

Yamazaki lacks cutting the two thin film integrated circuits.

Kawamura teaches:

limitations from claim 46, the method for manufacturing a thin film integrated circuit according to claim 3,

(see fig. 6 and 1B above) **wherein a thin film integrated circuit is formed by cutting the two thin film integrated circuits by a dicing, a scribing, or a laser cutting method,** limitation: scribing, col. 6, ln 10-22, col. 7, ln 31-67, col. 8, ln 1-16, col. 9, ln 1-41, fig. 1B and 6;

In fig. 6, Kawamura teaches a plurality of IC elements (1) are formed on a wafer (11). Antenna coils (3) are formed on top of the IC elements. The wafer is scribed to form individual IC elements as shown in fig. 1B.

Kawamura provides motivation in col. 9, ln 1-41.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Kawamura's invention with Yamazaki and Jurisch's invention would have been beneficial because the IC elements each formed integrally with the coil can be manufactured with high efficiency at lower manufacturing cost when compared with the case where the individual coils are each formed on the individual IC elements, respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHELE FAN whose telephone number is (571)270-7401. The examiner can normally be reached on M-F from 8 am to 4 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Unit 2823

3 February 2009

/M. F./

Examiner, Art Unit 2823